

In the Claims:

Please amend claims 5, 8 and 11-13, and add new claims 16-21 as indicated in the following listing, which replaces all prior versions.

1. (Previously presented) Method for operating an array of nonvolatile charge trapping memory devices, comprising:
before block erasing the array by discharging substantially all of the non-volatile charge trapping memory devices of the array,
block programming the array by charging substantially all of the non-volatile charge trapping memory devices of the array.
2. (Previously presented) Method according to claim 1, furthermore comprising after the erase operation programming some of the non-volatile memory devices of the array depending on data content to be stored in the non-volatile memory devices of the array.
3. (Previously presented) Method according to claim 2, furthermore comprising reading the data content stored in a non-volatile memory device of the array, wherein for reading the data content stored in a non-volatile memory device of the array at least one further non-volatile memory device having a dielectric charge trapping layer is used as reference cell which is programmed and erased for a block programming and block erase, respectively, of the non-volatile memory devices in the array.
4. (Previously presented) Method according to claim 3, wherein the memory devices of the array together function as reference cells.
5. (Currently amended) An electrical device comprising
an array of non-volatile charge trapping memory devices, and
a memory control arranged to
~~means for~~ control block programming the array by charging substantially all of the non-volatile charge trapping memory devices of the array,

~~means for~~ control block erasing the array by discharging substantially all of the programmed non-volatile charge trapping memory devices of the array, and

control ~~means for controlling~~ the array of non-volatile charge trapping memory devices such that before block erasing of substantially all of the non-volatile memory devices of the array, substantially all of the non-volatile memory devices of the array are block programmed.

6. (Previously presented) An electrical device according to claim 5, wherein the non-volatile memory device comprises a transistor having a channel and a control gate, a dielectric charge trapping layer being located between the channel and the control gate.

7. (Previously presented) An electrical device according to claim 5, the array being provided with at least one non-volatile memory device for use as a reference cell in a sense amplifier.

8. (Currently amended) An electrical device according to claim 7, the array comprising ~~means for~~ circuitry arranged to program programming and erase erasing the reference cell for a block-programming and block-erasing respectively of the non-volatile memory devices in the array.

9. (Previously presented) An electrical device according to claim 7, wherein the at least one reference cell is separate from the array.

10. (Previously presented) An electrical device according to claim 7, wherein the memory devices of the array together function as reference cells.

11. (Currently amended) An electrical device according to claim 7, comprising ~~means for comparing~~ circuitry arranged to compare a read current from a non-volatile memory device in the array with a read current from the reference cell.

12. (Currently amended) An electrical device according to claim 7, comprising ~~means for adapting~~ circuitry arranged to adapt a read current for reading the non-volatile memory devices in the array to the ageing of the reference cell.

13. (Currently amended) An electrical device according to claim 7, comprising ~~means for adapting~~ circuitry arranged to adapt a required control gate voltage for reading the non-volatile memory devices in the array depending on the ageing of the reference cell.

14. (Previously presented) An electrical device according to claim 5, wherein the array of non-volatile memory devices forms a non-volatile memory.

15. (Previously presented) A method according to claim 1, wherein the non-volatile memory devices of the array each include a dielectric charge trapping layer and wherein block programming the array by charging substantially all of the non-volatile charge trapping memory devices of the array includes trapping charge in the dielectric charge trapping layers.

16. (New) A method for use with programming an array of non-volatile charge trapping memory devices according to data content to be stored therein, the method comprising, prior to substantially every programming step:

block programming substantially all of the non-volatile charge trapping memory devices of the array; and

after the block programming step, block erasing substantially all of the non-volatile charge trapping memory devices of the array.

17. (New) The method of claim 16, further comprising programming a reference memory cell each time the block programming step is performed, and erasing the reference memory cell each time the block erasing step is performed, wherein the reference memory cell is a non-volatile charge trapping memory device.

18. (New) The method of claim 17, further comprising comparing a read current from a selected non-volatile memory device in the array with a read current from the reference memory cell.

19. (New) The method of claim 18, further comprising adapting the read current from the selected non-volatile memory device based on the read current from the reference memory cell.

20. (New) The method of claim 17, wherein the reference memory cell has a programming and erasing history that matches the block programming and blocking erasing history of the array.

21. (New) The method of claim 1, wherein the array is operated such that substantially none of the non-volatile charge trapping memory devices experiences two consecutive discharging cycles without experiencing an intermediate charging cycle.